DM621

12-CHANNELS PRE-PROGRAMMABLE CONSTANT CURRENT LED DRIVER

General Description

The DM621 is an innovative LED driver that integrates a new data transmit interface in order to eliminate control pins and accomplish most lighting applications easily. By the interaction of SIN and DCK, DM621 could be pre-programmed to set operating modes that involve GCK frequency division, PWM grayscale selection, inverse IOUT PWM signal, and GCK frequency selection. DM621 also provides the auto-latch function and incorporates a particular PWM method. The IOUT waveform is averagely divided into 16 sections in order to reduce the flickers and enhance the visual refresh rate. The DM621 could also be constructed as a PWM controller for LED drivers. In this case, resistors have to be connected at output pins to achieve this function.

This chip incorporates shift registers, data latches, 4x3-channel constant current circuitry with current value set by 3 external resistors, and 256/1024/4096/16384 gray level PWM function unit. Each channel provides a maximum current of 60mA. The maximum output sustaining voltage of 28V would make more serial LEDs possible. And DM621 also integrates an internal regulator to offer stable power supply voltage up to 18V adequate in the LED decorating applications.

Features

- 4 x 3(R/G/B) Output Channels
- 8/10/12/14-bits PWM grayscale Control
- Maximum Clock Frequency: 20MHz
- Constant Current Output: 5mA to 60mA
- Maximum Output Sustaining voltage: 28V
- Power Supply Voltage: 5V to 18V
- Average Separated IOUT PWM Waveform
- Auto-latch Function
- Serial Shift-In Architecture for Data of Grayscale, frequency Division and PWM bit number
- Incorporating internal GCK oscillator 10MHz
- Package: TSSOP24, QFN20
- Constant Current Matching: (Ta = 25°C、VDD = 12V)

  Chip-to-Chip: ± 6.0% (max)

  Bit-to-Bit: ± 3.0% (max)

Block Diagram

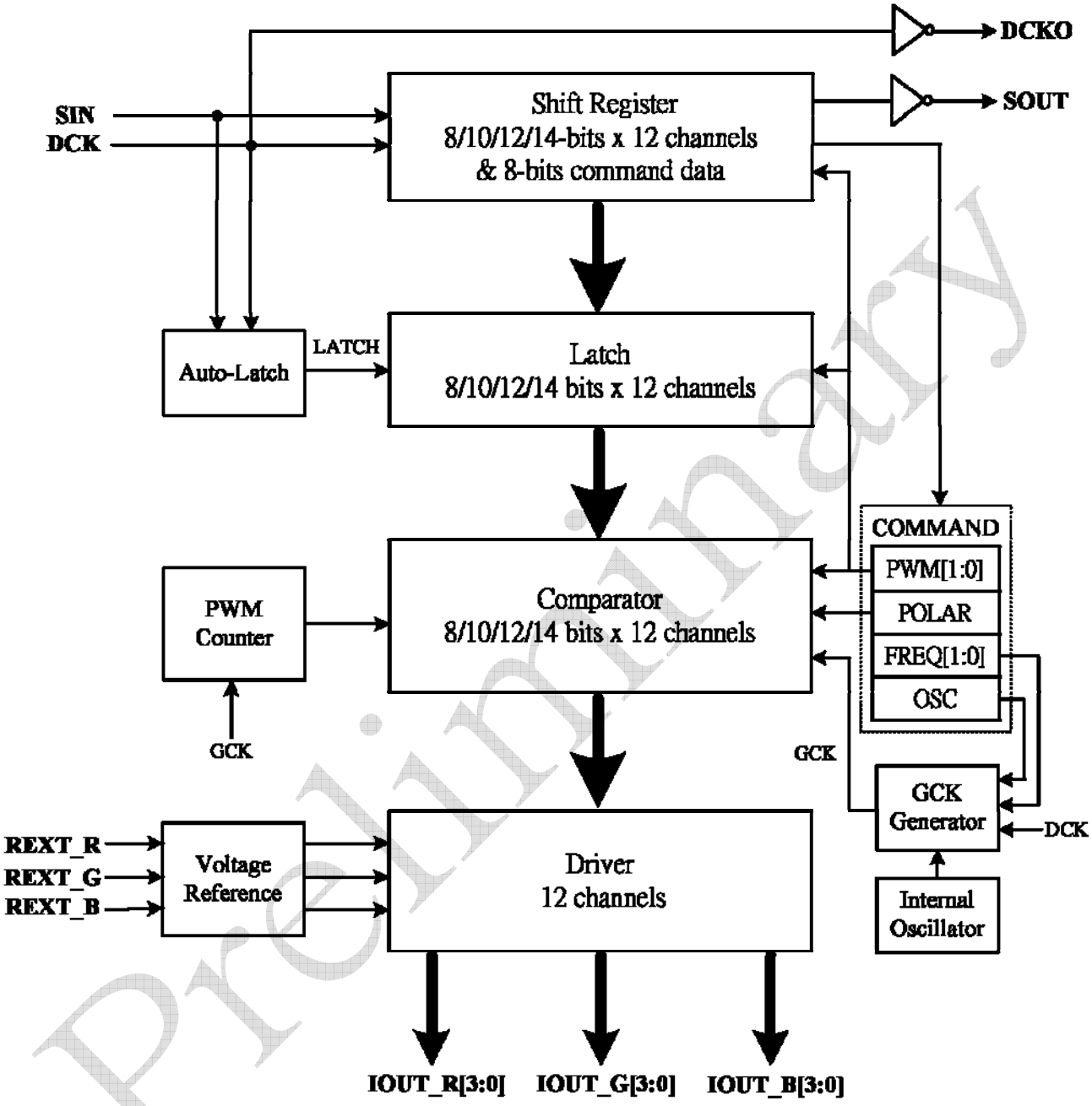


Figure 1. Functional Schematic of Whole Chip

The schematic of DM621 comprises of several fundamental units as shown in Figure1. The grayscale data and command data, transferred according to the synchronous clock DCK, are input into the SIN pin of DM621. Meanwhile, the combination of DCK and SIN data could produce the control signal of switching these two modes and achieve the auto-latch function.

Pin Description

PIN NAME	FUNCTION
VDD	Power supply terminal
DCK	Synchronous clock input for serial data. The input data of SIN is transferred at rising edges of DCK. It also could be used as GCK.
DCKO	Synchronous clock output
VSS_DR	Driver ground terminal
SIN	Serial input for grayscale data
SOUT	Serial output for grayscale data
REXT_R	External resistor connected between REXT and GND for driver current setting.
REXT_G	
REXT_B	
IOUT_R [3:0]	LED driver outputs
IOUT_G [3:0]	
IOUT_B [3:0]	

Pin Configuration (Top View)

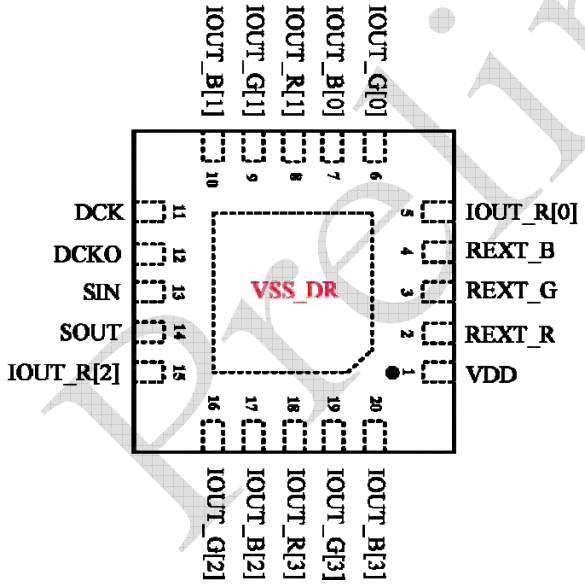


Figure 2. The Package of QFN20

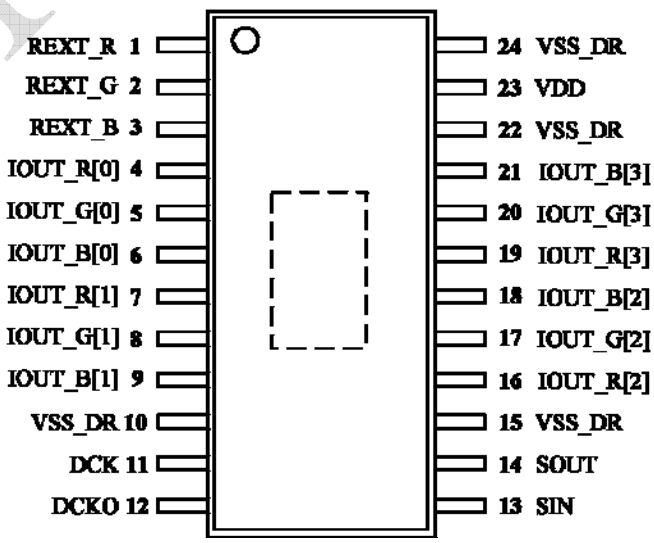


Figure 3. The Package of TSSOP24

Maximum Ratings (Ta = 25°C, $Tj_{(max)}$ = 150°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	18	V
Input Voltage	V_{IN}	5	V
Output Current	I_{OUT}	60	mA
Output Voltage	V_{OUT}	28	V
DCK Frequency	F_{DCK}	20	MHz
IGND Terminal Current	I_{GND}		mA
Power Dissipation	P_D	(QFN20); (SSOP24) (Ta=25°C)	W
Thermal Resistance	$R_{th(j-a)}$	(QFN20); (SSOP24)	°C/W
Operating Temperature	Topr	85	°C
Storage Temperature	Tstg	150	°C

Recommended Operating Condition

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	—	5	—	18	V
Output Voltage	V_{OUT}	—	—	—	28	V
Operating Temperature	T_{OPR}	—	-40	—	85	℃
Output Current	IOUT	OUT	5	—	60	mA
	I_{OH}	Serial-Output (SOUT/DCK_OUT)	—	—	2	mA
	I_{OL}	Serial-Output (SOUT/DCK_OUT)	—	—	-2	mA
Input Voltage	VIH	VDD=5V~17V	4	—	5	V
	VIL		0	—	1	

Electrical Characteristics (VDD = 12 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION		MIN.	TYP.	MAX.	UNIT
Input Voltage "H" Level	VIH	—		3	—	5	V
Input Voltage "L" Level	VIL	—		0	—	1	
Output Leakage Current	I_{OL}	VOUT = 26 V		—	—	1.0	uA
Output Current Skew (Bit-Bit)	∆Iout	VOUT = 1V	IOUT=10mA	—	—	±3	%
Output Current Skew (Chip-Chip)	∆Iout	VOUT = 1V	IOUT=10mA	—	—	±6	%
Output Voltage Regulation	I	Vout = 1.2V ~ 5.0V (% / Vout)	IOUT=10mA	—	0.1	0.5	% / V
Supply Voltage Regulation	% / VREF	VDD = 5V ~17V		—	0.5	1	% / V
Supply Current "OFF"	Idd (off)	REXT = OPEN, all outputs off		—	—	—	mA
		REXT = Ω (Iout=10mA), all outputs off		—	—	—	
Supply Current "ON"	Idd (on)	REXT = Ω (Iout=10mA), all outputs on		—	—	—	

Switching Characteristics (Ta = 25 °C unless otherwise noted)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
SOUT Propagation Delay ("L" to "H")	DCK to SOUT	$t_{PLH(sout)}$	VDD=12V VIH=5V VIL=GND Rext=Ω VLED=5V RL=120Ω CL=13pF	—	20	—	ns
SOUT Propagation Delay ("H" to "L")		$t_{PHL(sout)}$		—	20	—	ns
DCKO Propagation Delay ("L" to "H")	DCK to DCKO	$t_{PLH(DCKO)}$		—	20	—	ns
DCKO Propagation Delay ("H" to "L")		$t_{PHL(DCKO)}$		—	20	—	ns
Output Current Rise Time		tor		—	50	—	ns
Output Current Fall Time		tof		—	20	—	ns
SIN Setup Time		t_{setup}		—	1	—	ns
SIN Hold Time		t_{hold}		—	3	—	ns
Command Delay Time		t_{CMD}		—	10	—	ns
DCK Pulse Width		$T_{w(DCK)}$		—	25	—	ns
GCK Pulse Width		$T_{w(GCK)}$		—	25	—	ns

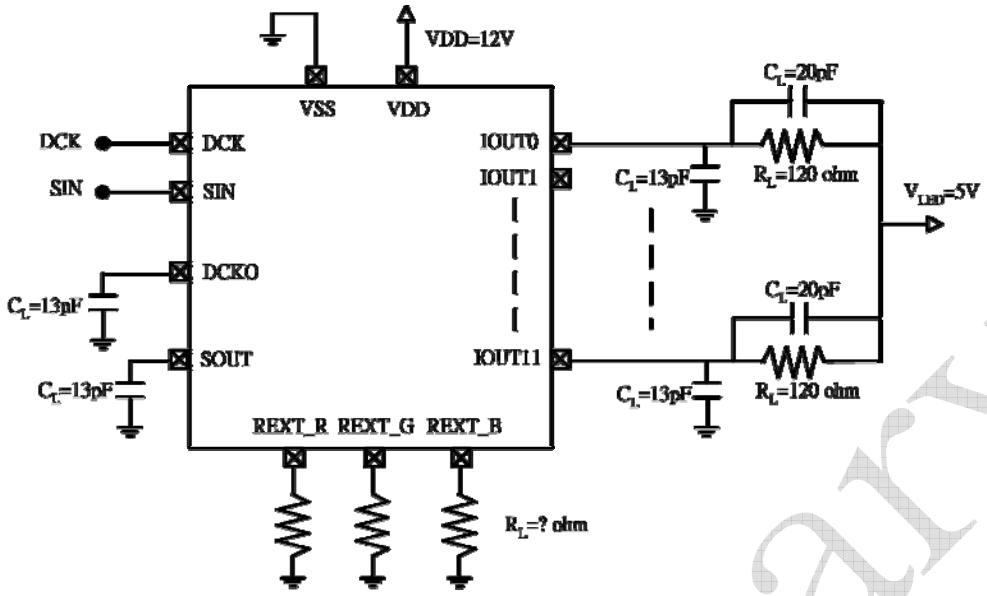


Figure 4. Measurement Architecture

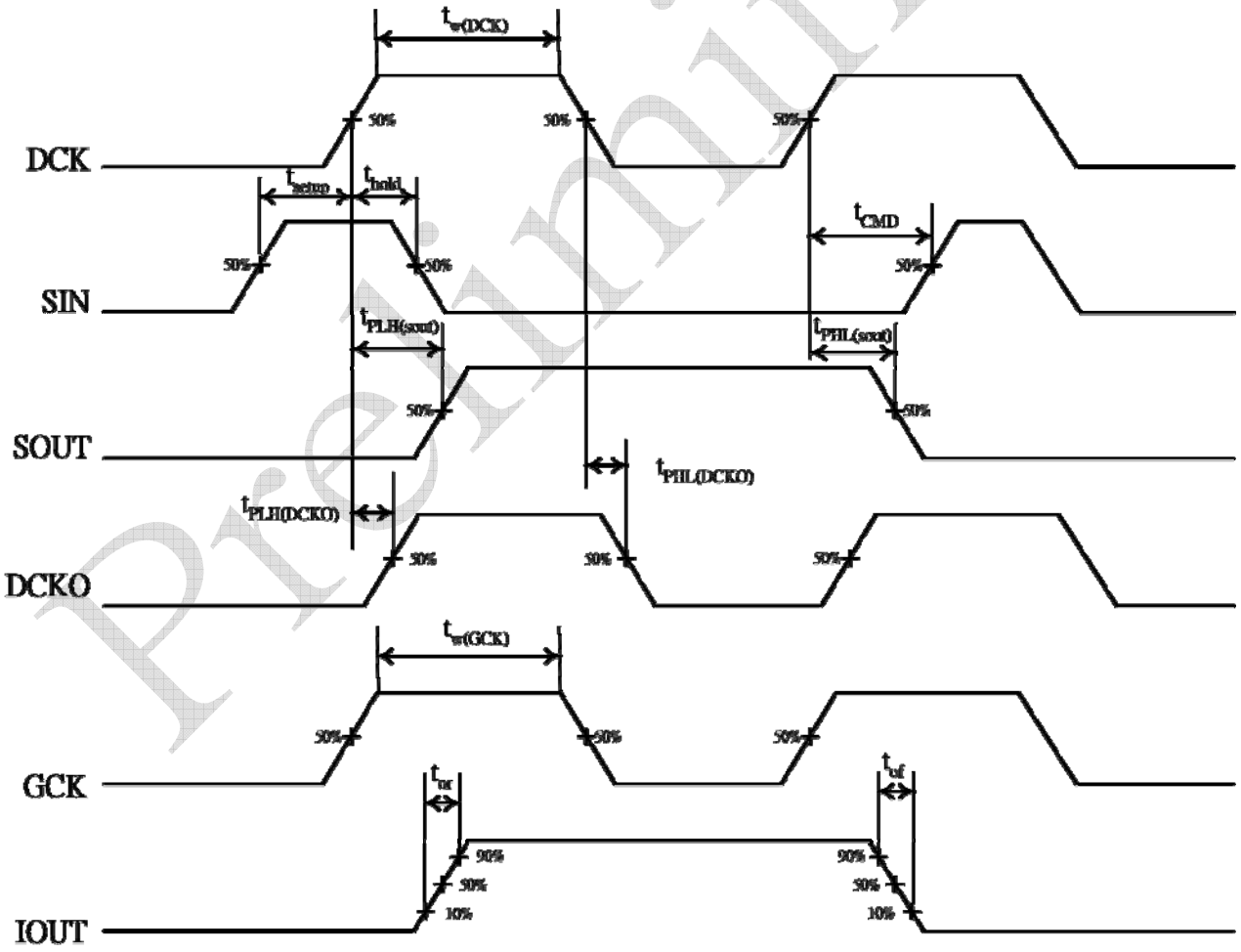


Figure 5. The Definitions of Parameters

Serial Shift-In Luminance Data (Shift Register Architecture)

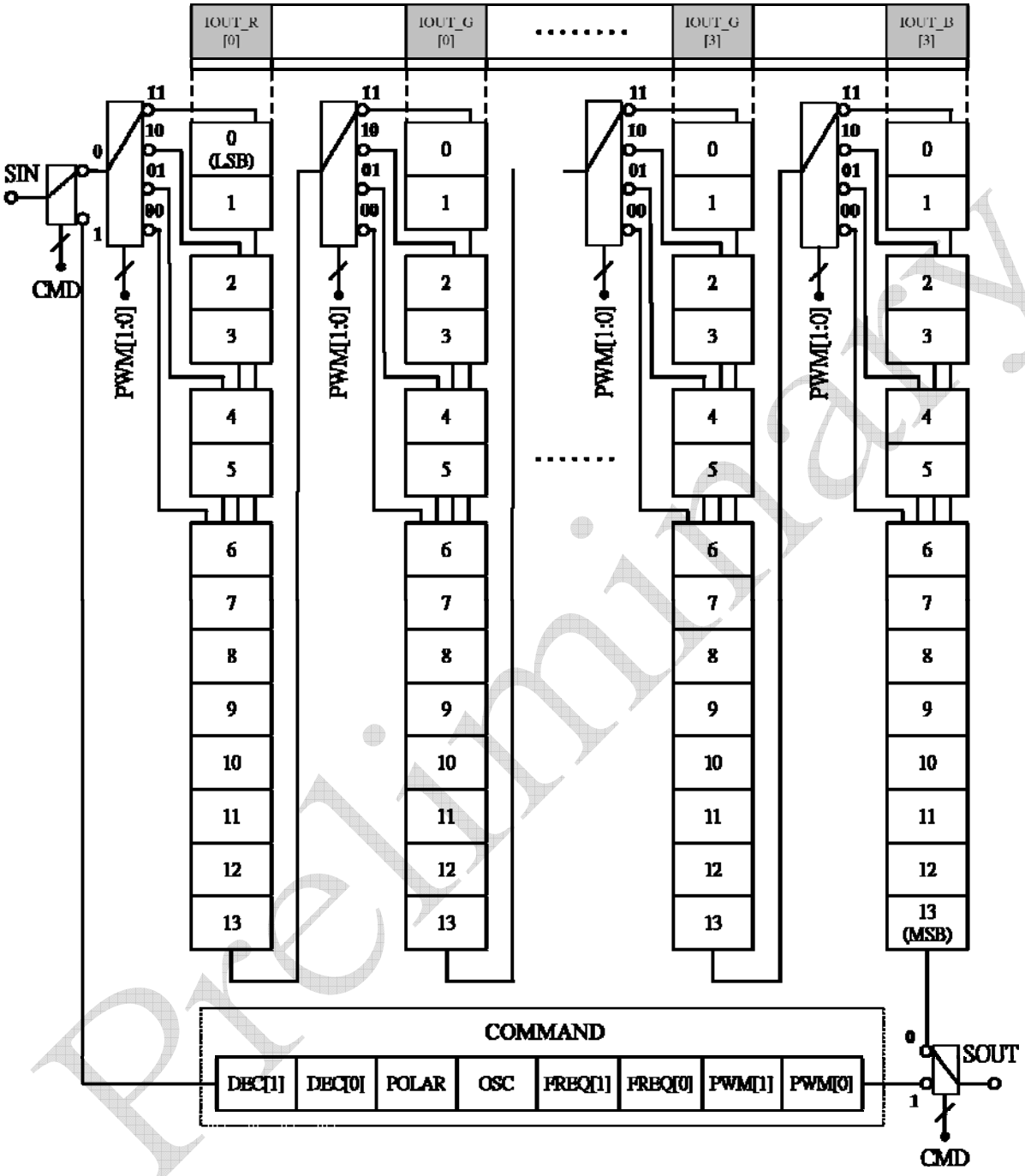


Figure 6. Serial Shift-In Luminance Data Structure

This serial shift (shift register) architecture follows a FIFO (first-in first-out) format.
The MSB (Most Significant Bit) data is the first data bit that shift into the driver.
The LSB (Least Significant Bit) data is the last bit in the data sequence.
And the PWM [1:0] command determines the data rate of each channel.

Average Separated PWM Waveform

The DM621 incorporates a new PWM method, hence the IOUT waveform demonstrates a very different characteristic compared to conventional PWM method. The IOUT waveform is averagely divided into 16 sections in a whole PWM period at each PWM mode. Furthermore, this progressive algorithm could efficiently reduce flickers and enhance the visual refresh rate.

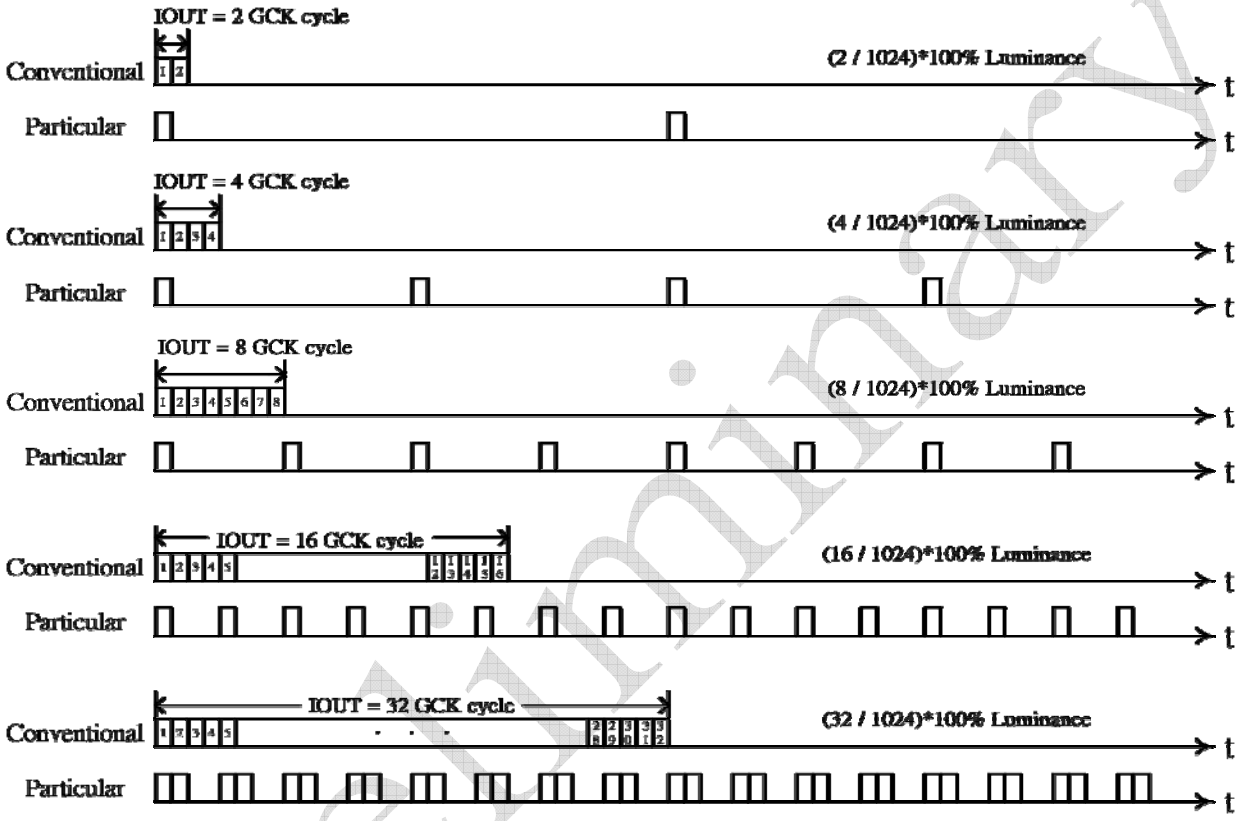


Figure 7. The Progressive PWM Method (1)

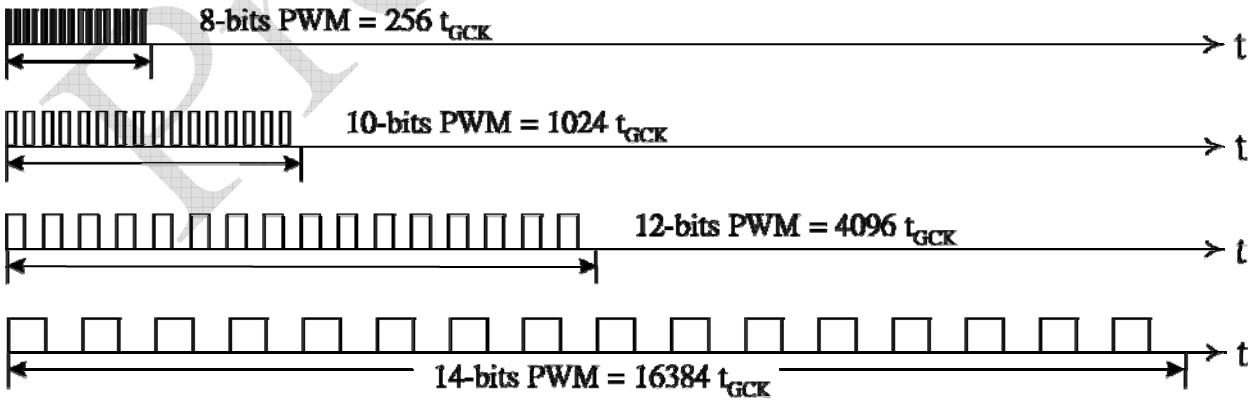


Figure 8. The Progressive PWM Method (2)

Command/Data Switching and Auto-latch Function

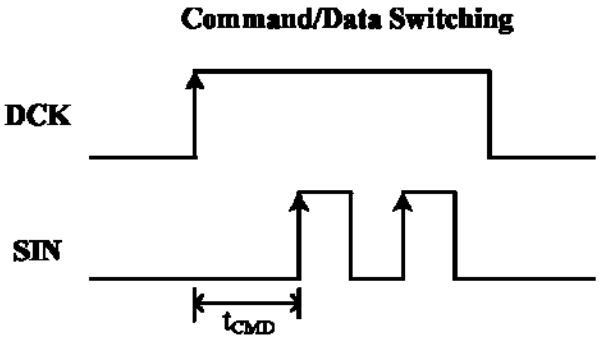


Figure 9(a). The Command/Data Method

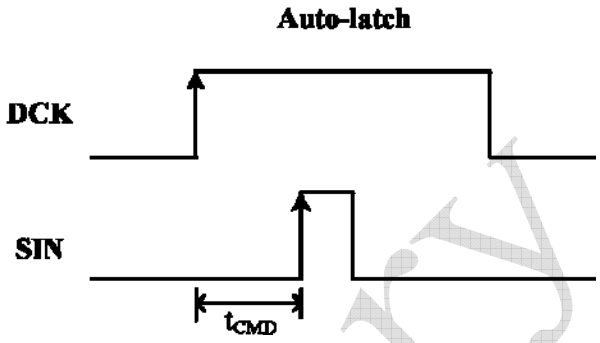


Figure 9(b). The Auto-latch Method

DM621 combines the signals of DCK and SIN to realize the Command/Data switching and Auto-latch function. When the area that DCK stays at high level includes two positive edges of SIN, DM621 would switch automatically to the command data mode, illustrated in Figure 9(a). At this time, 8-bits command data could be transmitted to set the operating condition adequate for different applications. As the process of command data transmission is accomplished, a latch signal would have to be executed by Auto-latch function. And this chip would latch command data into internal registers and return to the grayscale data mode as a latch instruction is executed. The Auto-latch function is realized by this method that the area that DCK stays at high level includes only one positive edge of SIN, illustrated in Figure 9(b). Note that the latch signal of command data and grayscale data could be completed according to the same Auto-latch process.

Both Command/Data switching and Auto-latch process would produce signals to control synchronously every serial DM621s. Therefore, each serial DM621 would enter the command mode and execute a latch instruction simultaneously. And DM621 also supports the internal synchronous clock for grayscale display. These characteristics would make great grayscale display possible. In this specific design, the smallest limitation of t_{CMD}, the time from the positive edge of DCK to the first positive edge of SIN, is 15ns in order to promise the correct command and grayscale data could be received.

Note that command data have to be transmitted to pre-programmed DM621s when the system is restarted because there are no EEPROM in this chip to save the command data and the grayscale data.

Command Data

COMMAND	FUNCTION
PWM [1:0]	8/10/12/14-bits PWM mode selection PWM [1:0] = 2'b00: 8-bits PWM count PWM [1:0] = 2'b01: 10-bits PWM count PWM [1:0] = 2'b10: 12-bits PWM count PWM [1:0] = 2'b11: 14-bits PWM count
FREQ [1:0]	GCK frequency division selection FREQ [1:0] = 2'b00: GCK=CLK FREQ [1:0] = 2'b01: GCK=CLK/2 FREQ [1:0] = 2'b10: GCK=CLK/4 FREQ [1:0] = 2'b11: GCK=CLK/8
OSC	GCK source selection OSC =1'b0: Internal oscillator (10MHz) OSC =1'b1: External DCK signal
POLAR	Inverse PWM data selection POLAR =1'b0: Normal PWM signal POLAR =1'b1: Inverse PWM signal
DEC [1:0]	Command Data Error Code (avoid interference) DEC [1:0] =2'b11: Command data is enable DEC [1:0] =others: Command data is disable

Timing Diagram

By the interaction of DCK and SIN data, DM621 could produce the internal CMD and LATCH signal to control the system automatically.

(Note*: CMD and LATCH are both the internal control signals)

(Note**: CMD="1" → command data mode, CMD="0" → grayscale data mode)

Command Data:

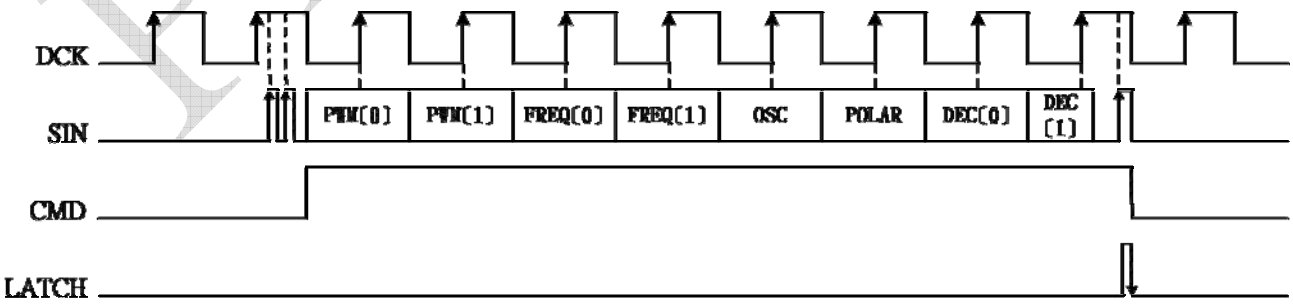


Figure 10. The timing diagram of command data

When there is two positive edges of SIN at DCK=”H”, DM621 produces CMD signal to switch to command data mode. Then users have to input 8bits command data to set the DM621 operating conditions described above. DM621 will latch command data into internal registers by incorporating one positive edge of SIN at DCK=”H”. Meanwhile, the CMD signal will return to zero.

Grayscale Data:

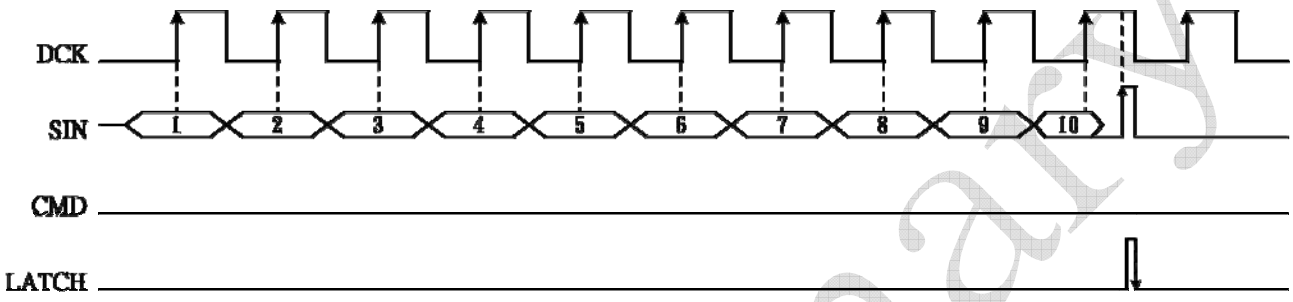


Figure 11. The timing diagram of grayscale data

According to the operating condition set at command mode, DM621 receives the 8bits/ 10bits/12bits/14bits PWM grayscale data. DM621 will latch grayscale data by incorporating one positive edges of SIN at DCK=”H”. Figure 11 is an illustration of 10-bits PWM grayscale data when the command data PWM [1:0]=2’b01.

Complete Data Transference:

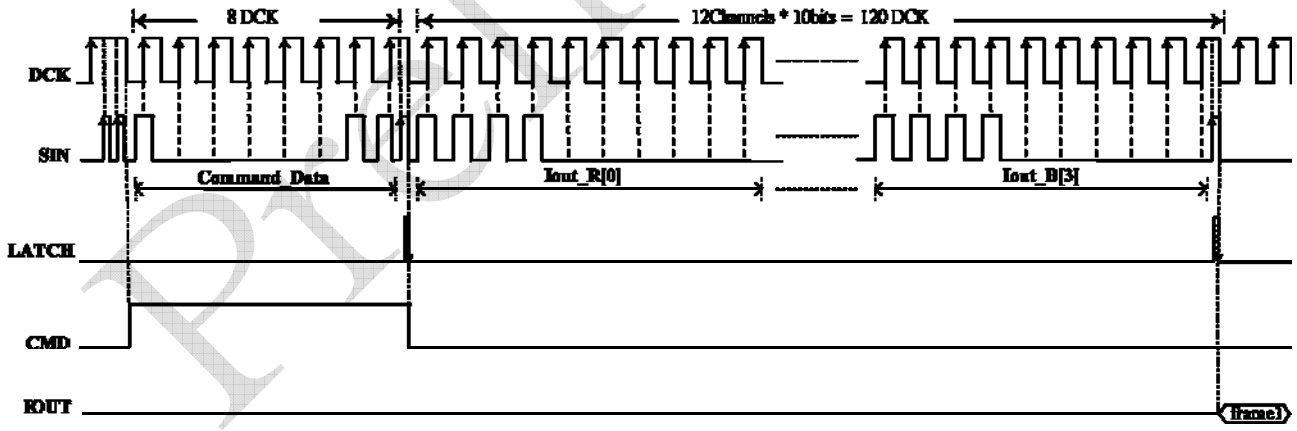


Figure 11. Detailed timing diagram of data transference

This is an illustration of the complete data transference of DM621. The command data sets the condition is 10-bits PWM mode, no GCK frequency division, no inverse PWM signal and the internal oscillator is utilized.

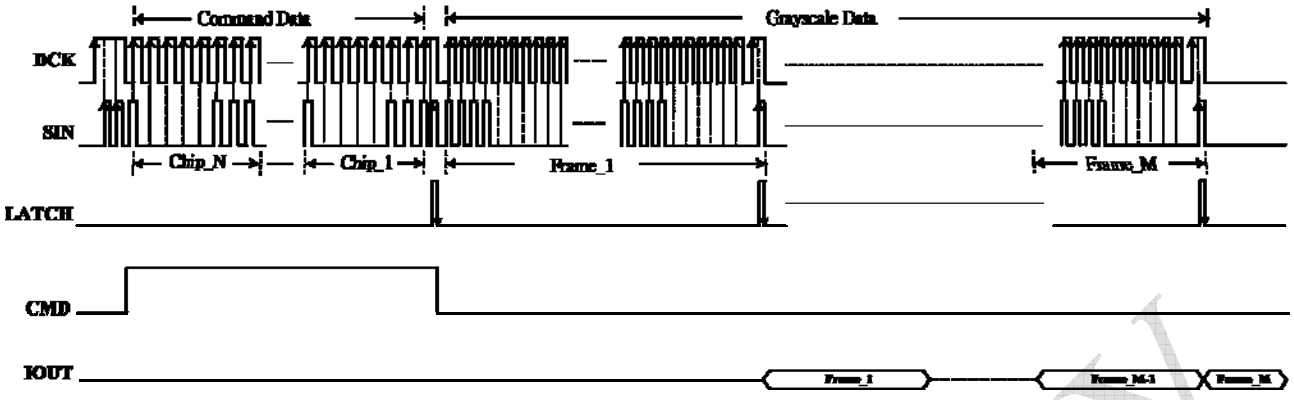


Figure 12. Timing diagram of serial data transference

If a lot of DM621s are connected in series, data could be transmitted according to the process illustrated in Figure 12. The Command/Data Switching function is executed just one time to set the operating conditions of all serial chips. After all command data and grayscale data are transmitted completely, an Auto-latch function is executed to latch data into internal registers.

Driver Output Current

Constant-current value of each output channel is set by an external resistor, which is connected between the REXT pin and GND. Varying the resistor value can adjust the current scale ranging from 5mA to 60mA. The reference voltage (Vrext) of REXT terminal is approximately 1.2V. The constant current formula is

$$IOUT(mA) = \frac{Vrext(V)}{\mathrm{Re}\,xt(k\Omega)} * 200 = \frac{1.2V}{\mathrm{Re}\,xt(k\Omega)} * 200$$

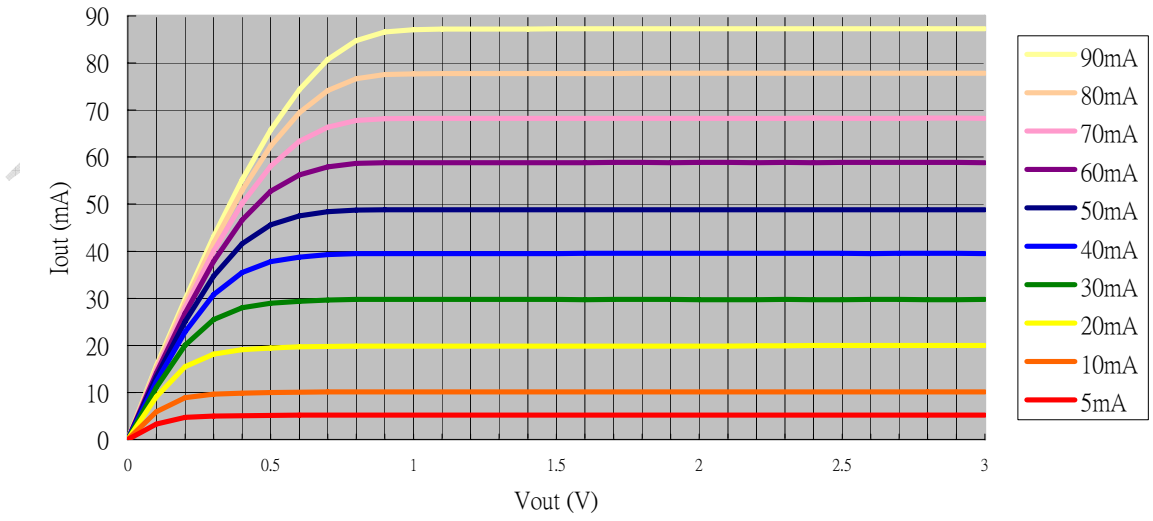
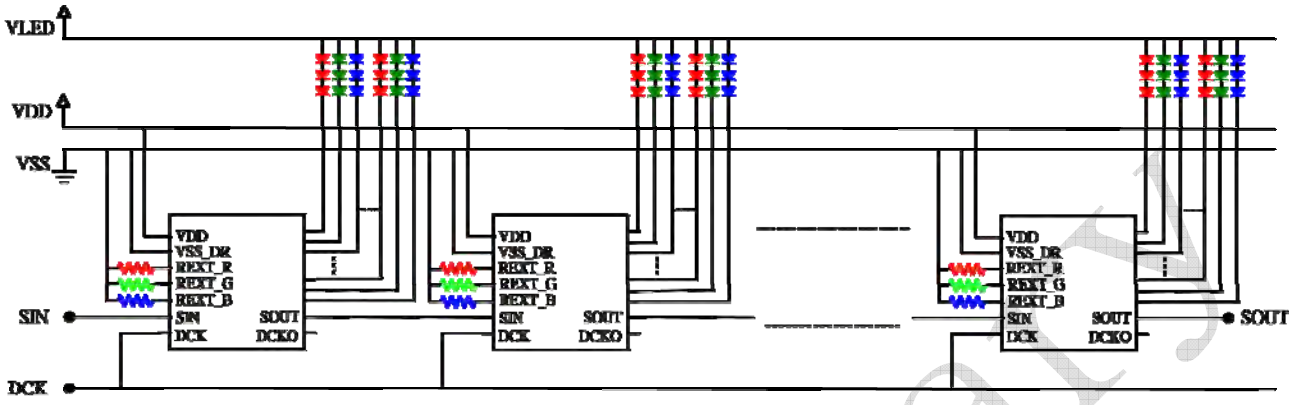


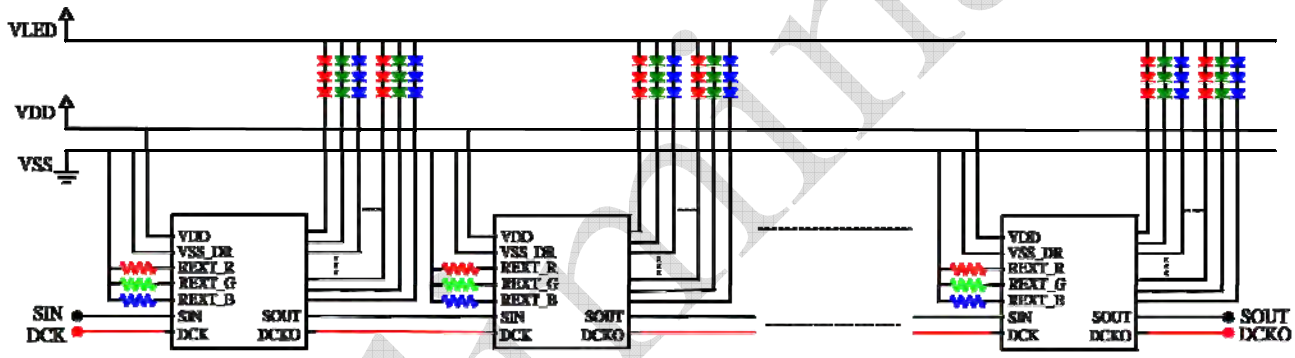
Figure 13. IOUT V.S. VOUT curve

Application Diagram

(1) DCK global connection (Figure 14):

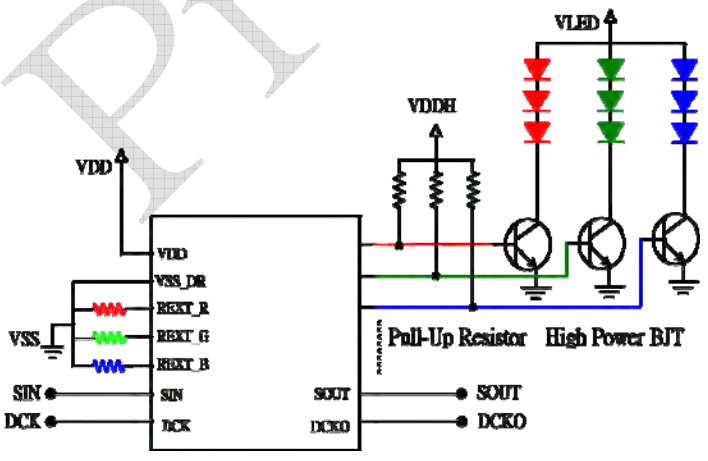


(2) DCK serial connection (Figure 15):



Just connected as the architecture illustrated above, DM621 could automatically produce the global latch and make serial data possible. The system just needs four lines (VDD, VSS, SIN, DCK) to realize the serial architecture.

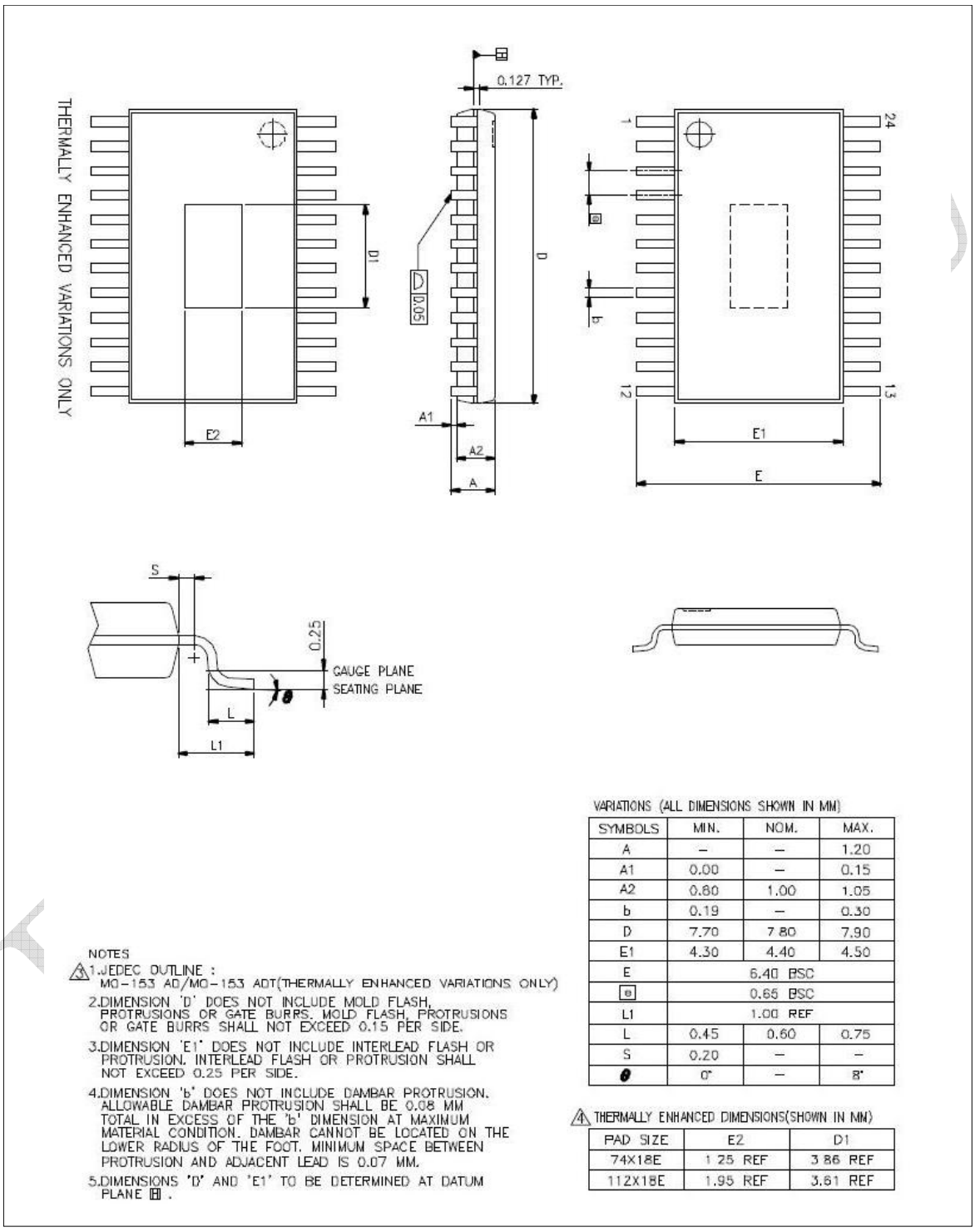
(3) PWM generator (Figure 16):



DM621 could be utilized as a PWM generator. In this case, DM621 will output inverse PWM signals by the POLAR command.

Package Outline

TSSOP24



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

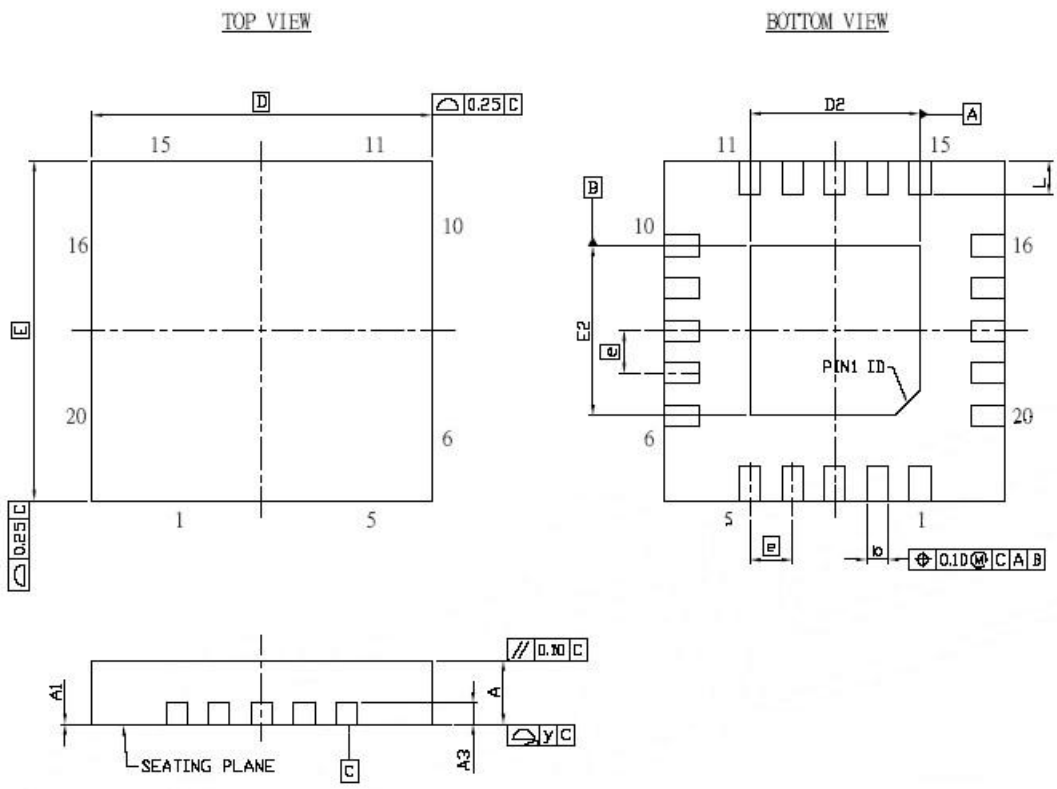
SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.00	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
D	7.70	7.80	7.90
E1	4.30	4.40	4.50
E		6.40 BSC	
e		0.65 BSC	
L1		1.00 REF	
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

NOTES
1. JEDEC OUTLINE : MO-153 AD/MO-153 ADT(THERMALLY ENHANCED VARIATIONS ONLY)
2. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3. DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.
5. DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE H.

THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	E2	D1
74X18E	1.25 REF	3.86 REF
112X18E	1.95 REF	3.61 REF

QFN20 (4mm*4mm)



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	27.56	29.53	31.50
A1	0	0.02	0.05	0	0.79	1.97
A3	0.203 REF			0 REF		
b	0.18	0.25	0.30	7.09	9.84	11.81
D	3.90	4.00	4.10	153.5	157.5	161.4
D2	1.90	2.00	2.10	74.8	78.7	82.7
E	3.90	4.00	4.10	153.5	157.5	161.4
E2	1.90	2.00	2.10	74.8	78.7	82.7
e	0.50 BSC			19.69 BSC		
L	0.30	0.40	0.50	11.81	15.74	19.69
y	0.08			3.15		