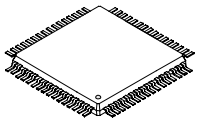
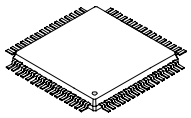
1/3 DUTY GENERAL-PURPOSE LCD DRIVER



QFP-64-14x14-0.8



LQFP-64-10 x 10-0.5

DESCRIPTION

The SC75823 is a general-purpose LCD driver that can be used for frequency display in microprocessor-controlled radio receives and in other display applications. In addition to being able to directly drive up to 156 LCD segments.

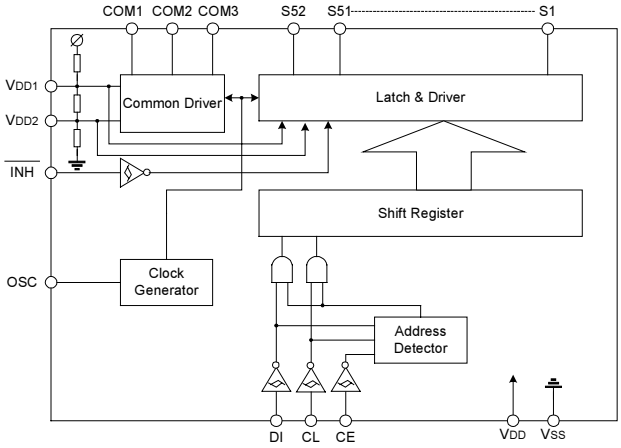
FEATURES

- Supports both 1/3 duty 1/2 bias and 1/3 duty 1/3 bias LCD drive of up to 156 segments under serial data control.
- Serial data input supports CCB format communication with the system controller.
- Serial data control of the power-saving mode based backup function and all the segments forced off function.
- High generality since display data is displayed directly without decoder intervention.
- The $\overline{INH}$ pin can force the display to the off state.
- The LCD drive bias voltage can be provided internally or externally.
- Power supply voltage: 4.5 to 6.0V

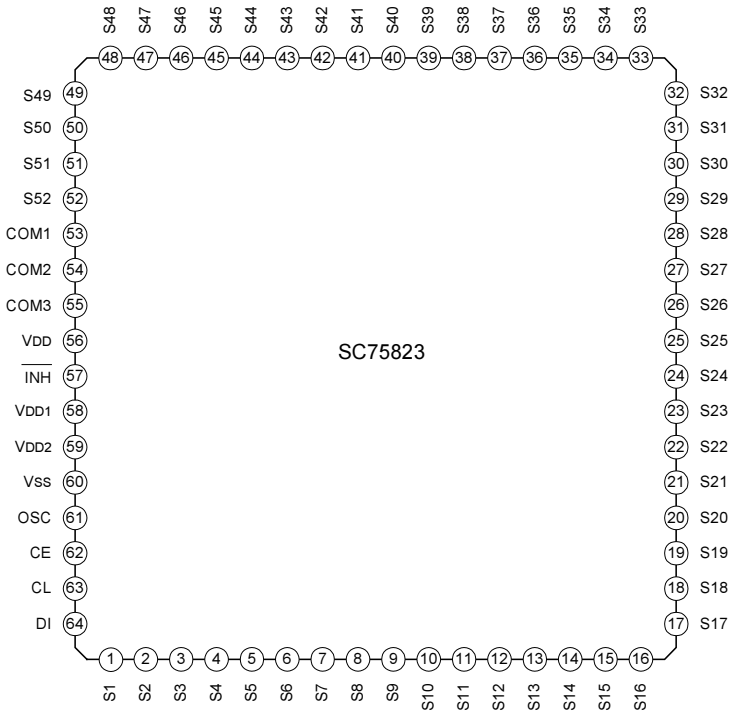
ORDERING INFORMATION

Device	Package
SC75823A	LQFP-64-10 X 10-0.5
SC75823B	QFP-64-14 X 14-0.8

BLOCK DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS (Tamb=25°C, V_{SS}=0 V)

Characteristics	Symbol	Value	Unit
Maximum Supply Voltage	V_{DDmax}	-0.3 to +6.5	V
Input Voltage	V_{IN1}	-0.3 to +6.5	V
	V_{IN2}	-0.3 to V_{DD}+0.3	V
Output Voltage	V_{OUT}	-0.3 to V_{DD}+0.3	V
Output Current	I_{OUT1}	300	μA
	I_{OUT2}	3	mA
Allowable Power Dissipation	P_{Dmax}	200	mW
Operating Temperature	T_{opr}	-40 to +85	°C
Storage Temperature	T_{stg}	-55 to 125	°C

ALLOWABLE OPERATING RANGE (Tamb=-40 to +85°C, V_{SS}=0V)

Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	V_{DD}	4.5		6.0	V
Input Voltage	V_{DD1}	V_{DD1}		2/3V_{DD}	6.0	V
	V_{DD2}	V_{DD2}		1/3V_{DD}	6.0	V
Input High level Voltage	V_{IH}	CE, CL, DI, $\overline{INH}$	4.0		6.0	V
Input Low Level Voltage	V_{IL}	CE, CL, DI, $\overline{INH}$	0		0.7	V
Recommended External Resistance	R_{OSC}	OSC		47		kΩ
Recommended External Capacitance	C_{OSC}	OSC		1000		pF
Guaranteed Oscillator Range	f_{OSC}	OSC	19	38	76	kHz
Data Setup Time	tds	CL, DI: figure 2	100			ns
Data Hold Time	tdh	CL, DI: figure 2	100			ns
CE Wait Time	tcp	CE, CL: figure 2	100			ns
CE Setup Time	tcs	CE, CL: figure 2	100			ns
CE Hold Time	tch	CE, CL: figure 2	100			ns
High-level Clock Pulse Width	tϕH	CL: figure 2	100			ns
Low-level Clock Pulse Width	tϕL	CL: figure 2	100			ns
Rise Time	tr	CE, CL, DI: figure 2		100		ns
Fall Time	tf	CE, CL, DI: figure 2		100		ns
$\overline{INH}$ Switching Time	t2	$\overline{INH}$, CE: figure 3	10			μs

ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input High Level Current	I_{IH}	CE, CL, DI, $\overline{INH}$; V_I=6V			5	μA
Input Low Level Current	I_{IL}	CE, CL, DI, $\overline{INH}$; V_I=0V	-5			μA
Oscillator Frequency	f_{OSC}	OSC;R_{OSC}=47kΩ, C_{OSC}=1000pF		38		kHz
Hysteresis Width	V_H	CE, CL, DI, $\overline{INH}$; V_{DD}=5V	0.3			V
Output High Level Voltage	V_{OH1}	S1 to S52; I_O=-20μA	V_{DD}-1.0			V
Output Low Level Voltage	V_{OL1}	S1 to S52; I_O=20μA			1.0	V
Output High Level Voltage	V_{OH2}	COM1 to COM3; I_O=-100μA	V_{DD}-1.0			V
Output Low Level Voltage	V_{OL2}	COM1 to COM3; I_O=100μA			1.0	V
Intermediate Level Voltage	V_{MID1}	1/2 bias, COM1 to COM3; I_O=±100μA	1/2V_{DD}±1.0			V
	V_{MID2}	1/3 bias, COM1 to COM3; I_O=±100μA	2/3V_{DD}±1.0			V

(To be continued)

(Continued)

Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Intermediate Level Voltage*	V_{MID3}	1/3 bias, COM1 to COM3; I_O=±100μA	1/3V_{DD}±1.0			V
	V_{MID4}	1/3 bias, S1 to S52; I_O=±20μA	2/3V_{DD}±1.0			V
	V_{MID5}	1/3 bias, S1 to S52; I_O=±20μA	1/3V_{DD}±1.0			V
Supply Current	I_{DD1}	Power saving mode			5	μA
	I_{DD2}	f=38kHz, 1/2 bias, V_{DD}=5V		400	800	μA
	I_{DD3}	f=38kHz, 1/3 bias, V_{DD}=5V		300	600	μA
	I_{DD2}	f=38kHz, 1/2 bias, V_{DD}=6V		650	1300	μA
	I_{DD3}	f=38kHz, 1/3 bias, V_{DD}=8V		580	1200	μA

Note: * Except the bias voltage generation divider resistors that are built into V_{DD1} and V_{DD2}.(see figure 1)

Figure 1

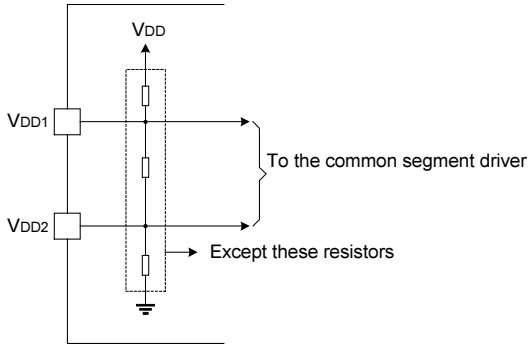
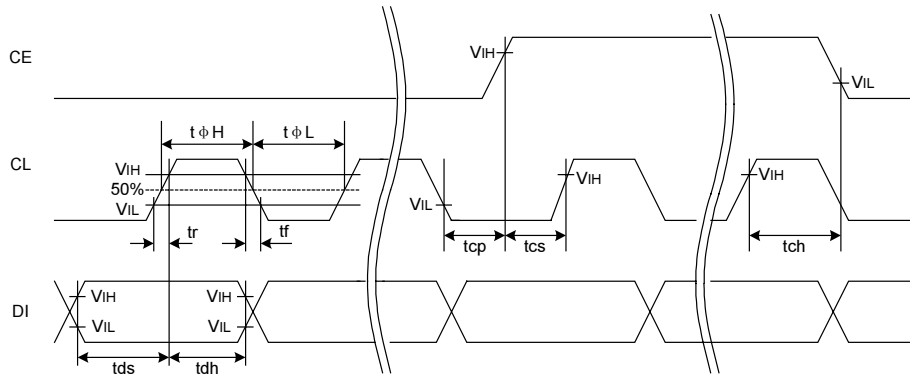
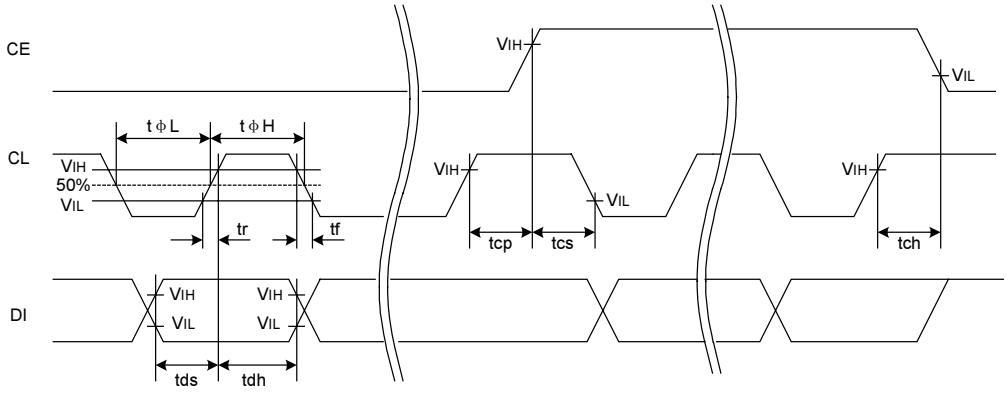


Fig 2

1.When CL is stopped at the low level



2.When CL is stopped at the high level



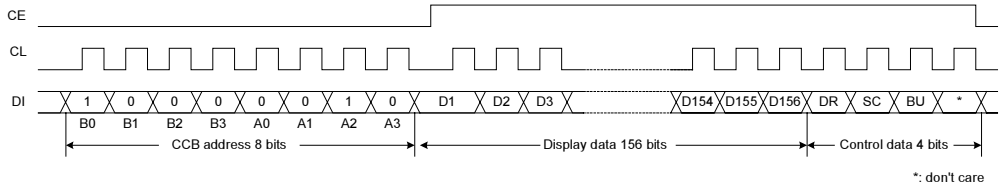
PIN DESCRIPTION

Pin No	Symbol	I/O	Description	
1-52	S1 to S52	O	Segment outputs for displaying the display data transferred by serial data input.	
53	COM1	O	Common driver outputs. The frame frequency f_O is given by: $f_O=(f_{OSC}/384)Hz$	
54	COM2			
55	COM3			
61	OSC	I/O	Oscillator connection An oscillator circuit is formed by connecting an external resistor and capacitor to this pin.	
62	CE	I	Serial data transfer inputs. These pins are connected to the control microprocessor.	CE: chip enable
63	CL			CL: synchronization clock
64	DI			DI: transfer data
57	$\overline{INH}$	I	Display off control input $\overline{INH}$ =low (V_{SS})……Display forced off (S1 to S52, COM1 to COM3=low) $\overline{INH}$ =high (V_{DD})……Display on note that serial data transfers can be performed when the display is forced off.	
58	V_{DD1}	I	Used for the 2/3 bias voltage when bias voltage are provided externally. Connect to V_{DD2} when 1/2 bias is used.	
59	V_{DD2}	I	Used for the 1/3 bias voltage when bias voltage are provided externally. Connect to V_{DD1} when 1/2 bias is used.	
56	V_{DD}	--	Power supply. Provide a voltage of between 4.5 and 6.0V	
60	V_{SS}	--	Ground. Connect this pin to the system ground.	

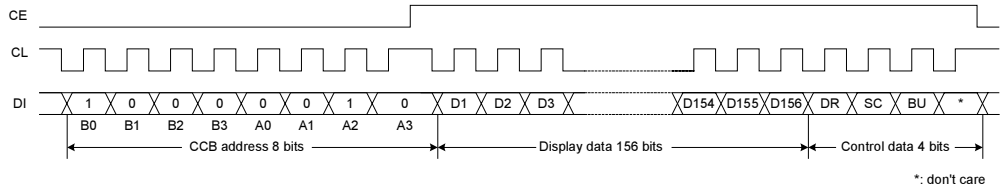
FUNCTION DESCRIPTION

Serial data transfer format

1. When CL is stopped at the low level



2. When CL is stopped at high level



- CCB address…….41H
- D1 to D156…….Display data

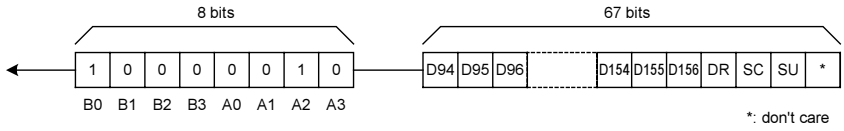
  Dn (n=1 to 156)=1……..Display on

  Dn (n=1 to 156)=0……..Display off
- DR……1/2-bias drive or 1/3-bias drive switching control data
- SC……Segments on/off control data
- BU……Normal mode/power-saving mode control data

Serial data transfer examples

- When 63 segments are used

63 bits is display data (D94 to D156) must be sent.



Control data function

1. DR: 1/2-bias drive or 1/3-bias drive switching control data

This control data selects either 1/2-bias drive or 1/3-bias drive.

DR	Drive type
0	1/2-bias drive
1	1/3-bias drive

2. SC: segments on/off control data

This control data bit controls the on/off state of the segments.

SC	Display state
0	On
1	Off

However, note that when the segments are turned off by setting SC to 1, the segments are turned off by outputting segment off waveforms from the segment output pins.

3. BU: Normal mode/power-saving mode control data

BU	Mode
0	Normal mode
1	Power-saving mode. In this mode the OSC pin oscillator is stopped and the common and segment pins output VSS levels.

Display data to segment output pin correspondence

Segment output pin	COM3	COM2	COM1	Segment output pin	COM3	COM2	COM1
S1	D1	D2	D3	S27	D79	D80	D81
S2	D4	D5	D6	S28	D82	D83	D84
S3	D7	D8	D9	S29	D85	D86	D87
S4	D10	D11	D12	S30	D88	D89	D90
S5	D13	D14	D15	S31	D91	D92	D93
S6	D16	D17	D18	S32	D94	D95	D96
S7	D19	D20	D21	S33	D97	D98	D99
S8	D22	D23	D24	S34	D100	D101	D102
S9	D25	D26	D27	S35	D103	D104	D105
S10	D28	D29	D30	S36	D106	D107	D108
S11	D31	D32	D33	S37	D109	D110	D111
S12	D34	D35	D36	S38	D112	D113	D114
S13	D37	D38	D39	S39	D115	D116	D117
S14	D40	D41	D42	S40	D118	D119	D120
S15	D43	D44	D45	S41	D121	D122	D123
S16	D46	D47	D48	S42	D124	D125	D126
S17	D49	D50	D51	S43	D127	D128	D129
S18	D52	D53	D54	S44	D130	D131	D132
S19	D55	D56	D57	S45	D133	D134	D135

（To be continued）

(Continued)

Segment output pin	COM3	COM2	COM1	Segment output pin	COM3	COM2	COM1
S20	D58	D59	D60	S46	D136	D137	D138
S21	D61	D62	D63	S47	D139	D140	D141
S22	D64	D65	D66	S48	D142	D143	D144
S23	D67	D68	D69	S49	D145	D146	D147
S24	D70	D71	D72	S50	D148	D149	D150
S25	D73	D74	D75	S51	D151	D152	D153
S26	D76	D77	D78	S52	D154	D155	D156

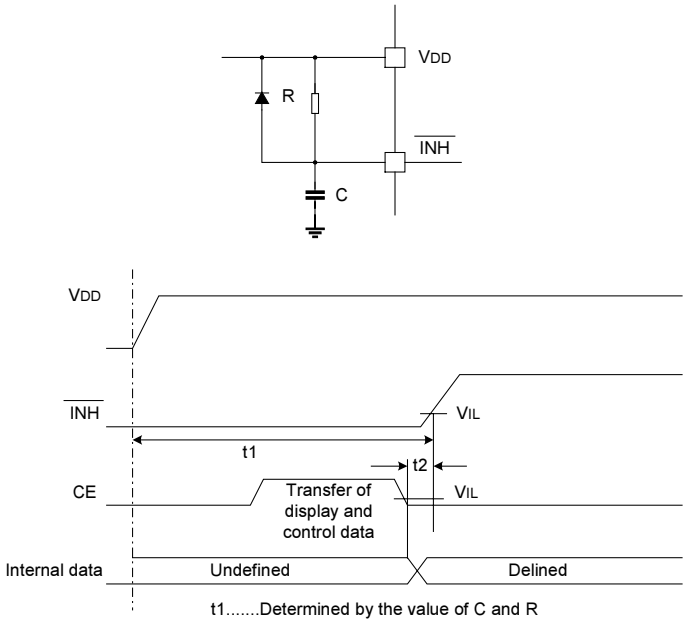
For example, the table below lists the segment output states for the S11 output pin.

Display data			Segment output pin (S11) state
D31	D32	D33	
0	0	0	The LCD segments corresponding to COM1 to COM3 are off.
0	0	1	The LCD segments corresponding to COM1 is on.
0	1	0	The LCD segments corresponding to COM2 is on.
0	1	1	The LCD segments corresponding toCOM1 and COM2 are on.
1	0	0	The LCD segments corresponding to COM3 is on.
1	0	1	The LCD segments corresponding to COM1 and COM3 are on.
1	1	0	The LCD segments corresponding to COM2 and COM3 are on.
1	1	1	The LCD segments corresponding to COM1 to COM3 are on

$\overline{\text{INH}}$ and display control

Since the LSI internal data (D1 to D156, DR, SC and BU) is undefined when power is first applied, the display is off (S1 to S52, COM1 to COM3= low) by setting the $\overline{\text{INH}}$ pin low at the same as power is applied. Then, meaningless display at the power-on can be prevented by transferring serial data from the controller while the display is off and setting $\overline{\text{INH}}$ pin high after the transfer completes.(see figure3).

Figure 3

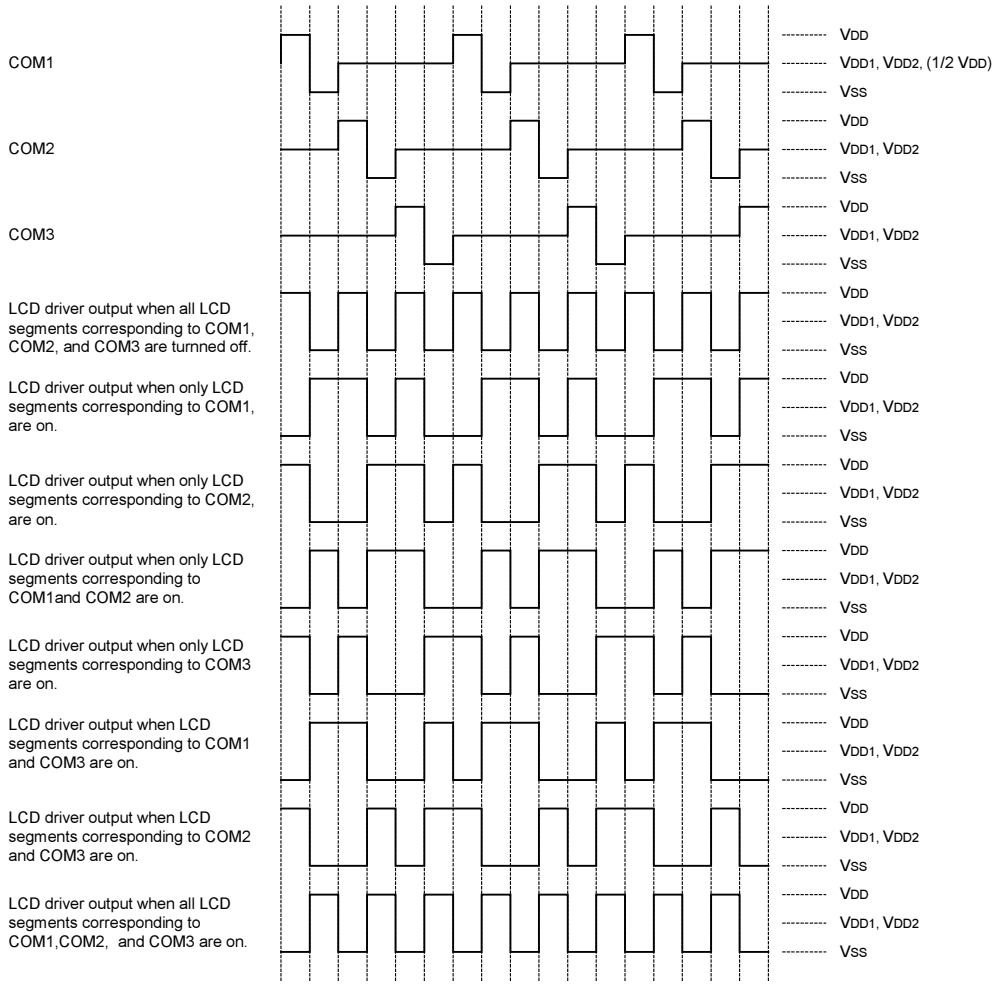


t1.....Determined by the value of C and R

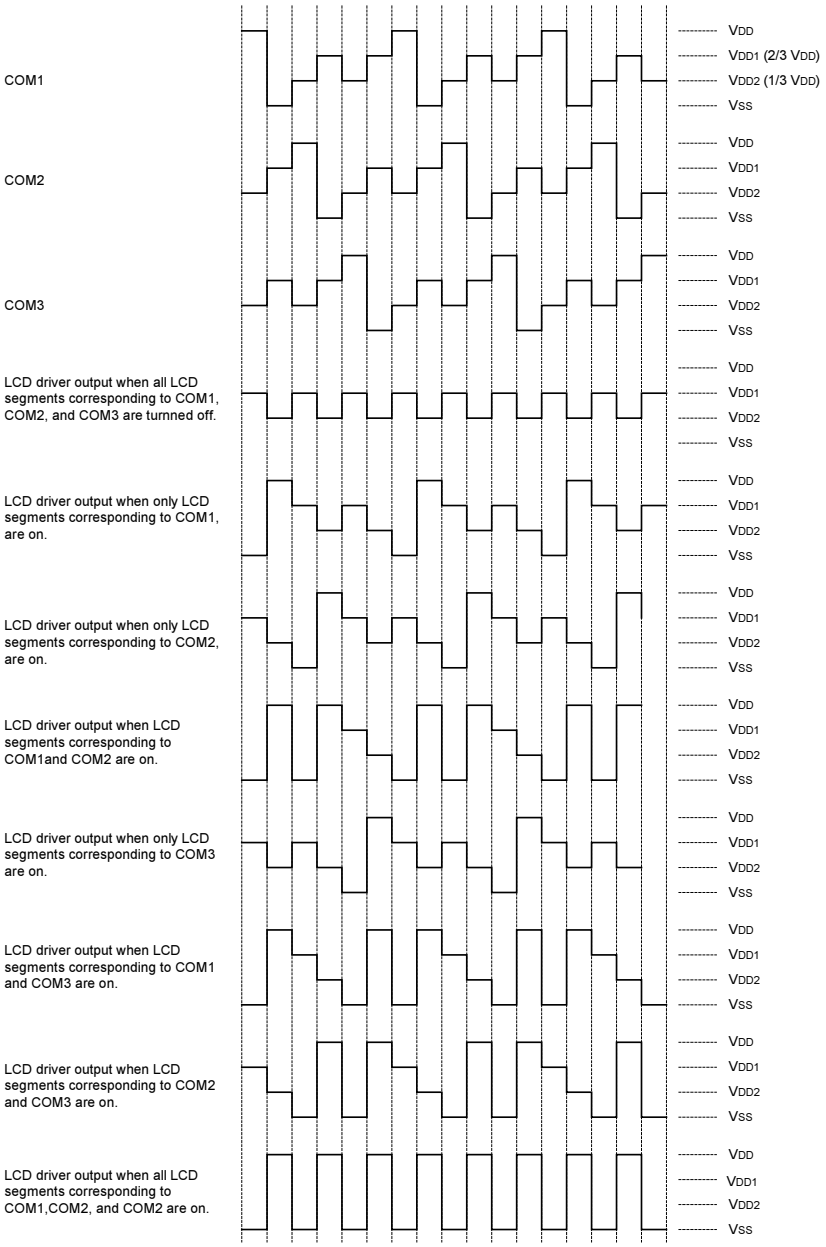
t2.....10 μ s(minimum)

TIMING DIAGRAM

1/2 Bias , 1/3 Duty Drive Technique

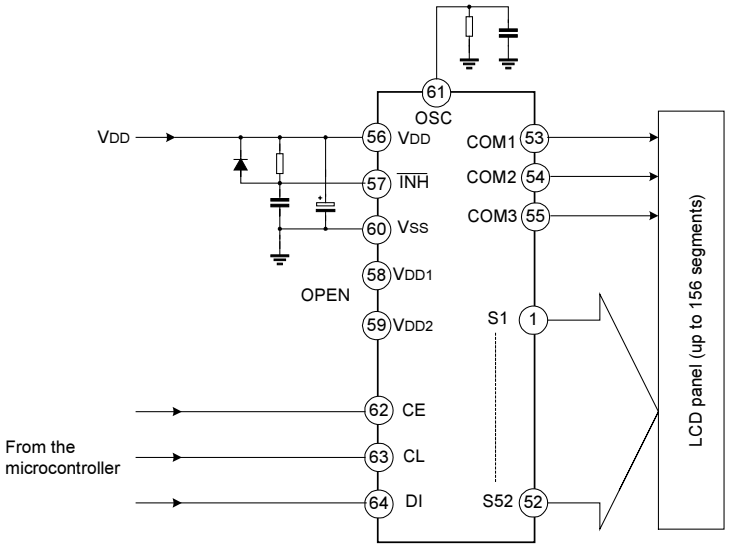


1/3 Bias, 1/3 Duty Drive Technique



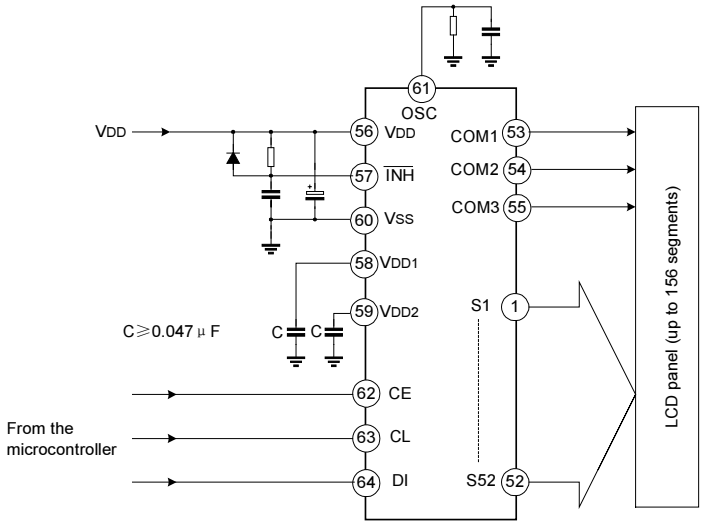
TEST CIRCUIT1

1/3 Bias (for use with small panels)



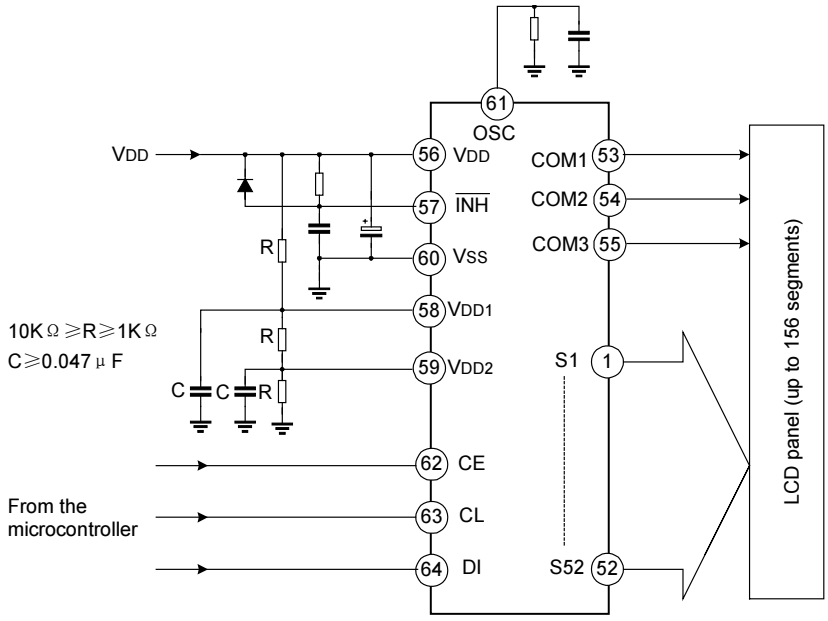
TEST CIRCUIT2

1/3 Bias (for use with normal size panels)



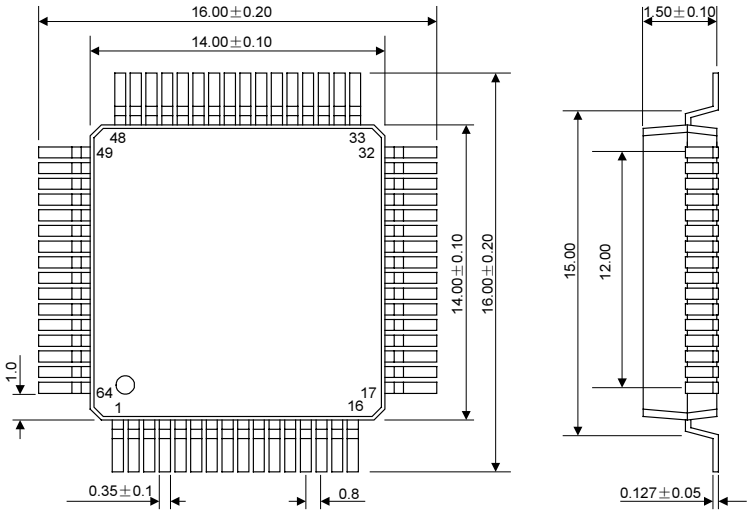
TEST CIRCUIT3

1/3 Bias (for use with large panels)



PACKAGE OUTLINE

QFP-64-14 x 14-0.8 UNIT: mm



LQFP-64-10x10-0.5 UNIT: mm